**VLSI Basic Concepts for Digital Standard Cell Library**

1) **Logical States**

* L = 0 🡪 Low Logic Level
* H = 1 🡪 High Logic Level
* Z 🡪 High Impedance State
* LH 🡪 Low to High Transition
* HL 🡪 High to Low Transition
* X = Unknown 🡪 Either High or Low Logic Level

2) **Voltage Transfer Characteristics (VTC)**

* DC functional dependence between input and output voltages.

3) **Switching Point Voltage**

* A point on VTC curve where input and output voltages are equal.

4) **Noise Margin**

5) **Rise Time**

* Duration time from 10% to 90% of .

6) **Fall Time**

* Duration time from 90% to 10% of .

7) **Rise Propagation Delay**

* Duration time from 50% of to 50% of in low to high transition.

8) **Fall Propagation Delay**

* Duration time from 50% of to 50% of in high to low transition.

9) **Setup Time**

* The minimum period of time in which the input data to a flip-flop or latch must be stable before the clock active edge occurs.

10) **Hold Time**

* The minimum period of time in which the input data to a flip-flop or latch must remain stable after the occurrence of clock active edge.

11) **Driving Strength**

* The maximum load capacitance that a logic cell output pin can drive.

12) **Digital Standard Cell Library**

* Purpose 🡪 Optimizing the main characteristics of integrated circuits.
* Contains both Combinational and Sequential logic cells.
* Includes logic cells with different threshold voltages. 🡪 Usage in Low Power Design
* HVT 🡪 High Threshold Voltage
* RVT 🡪 Regular Threshold Voltage
* LVT 🡪 Low Threshold Voltage
* Formats of Deliverable Files
* Synthesis 🡪 **.db** and **.lib**
* Verilog and VHDL Simulation Models 🡪 **.v** and **.vhd**
* TetraMAX Verilog Models 🡪 **.tv**